

Dynamic PCI-Bus Pre-Fetch with Separate Counters for Commands of Different Data-Transfer Lengths

Abstract

A Peripheral Component Interconnect (PCI) bridge between two buses prefetches read data into a cache. The number of cache lines to prefetch is predicted by a prefetch counter. One prefetch counter is kept for each type of memory-read command: basic memory-read (MR), memory-read-line (MRL) that reads a cache line, and memory-read-multiple (MRM) that reads multiple cache lines. For each type of read command, counters are kept of the number of completed commands, bus-disconnects (indicating under-fetch), and master-discard of data (indicating over-fetch). After a predetermined number of execution of each type of command, the command's prefetch counter is incremented if under-fetching occurred, or decremented if over-fetching occurred, as indicated by the disconnect and discard counters for that type of read command. The command's other counters are reset.

Prefetching is optimized for each type of read command. MRM can prefetch more data than MRL or MR.